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Supporting Information

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Ink-Jet Printed CMOS Electronics from Oxide Semiconductors

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Contents:

A. Additional experimental information

Device preparation:

The FETs were built on commercially available thermally oxidized Si wafers with 200 nm SiO_2 on top. The FET design was simple in-plane transistor structure where the gate (G), source (S), drain (D) electrodes were placed at the same plane of the substrate. Sputtered chromium (10 nm)/platinum (30 nm) were used as the electrode materials. The passive structures were patterned using e-beam lithography with PMMA as photoresist. On the patterned structures, the precursor solutions were printed and dried at 150 °C for 2-3 min and subsequently annealed at 400 ˚C for 2 hr. After the annealing step, a composite solid polymer electrolyte was printed to be used as the gate insulator and allowed to dry slowly at ambient conditions. The printing parameters were similar in both cases; applied voltage to the piezo element was 40 V, jetting frequency was 5 kHz, meniscus set point was 5.0, and the Dimatix standard waveform was used to print the structures.

Preparation of composite solid polymer electrolyte:

Necessary amount of $LiClO_4$ was dissolved in propylene carbonate (PC) at room temperature. In parallel, another solution was prepared by dissolving polyvinyl alcohol (PVA) in dimethyl sulfoxide (DMSO) at 90 °C for 1 hr. After both turned into transparent, homogeneous solutions, they were mixed together thoroughly under continuous stirring until a completely homogeneous solution was obtained. The weight ratio of PVA:$LiClO_4$:PC was optimized and kept constant at 30.7.63; while the DMSO was taken 6 times the weight of the all other ingredients together.

B. Calculated average crystallite size of indium oxide and copper oxide films vs. annealing temperatures

To calculate the crystallite size, first the instrumental broadening has been estimated using a standard corundum (Al_2O_3) sample. The volume weighted average crystallite size of the In_2O_3 film annealed at different temperatures, CuO film is calculated using equation S1 and S2 and the data is summarized in table S1.[S1]

$$\beta_{calc}^2 = \beta_{meas}^2 - \beta_{inst}^2 \quad \text{(S1)}$$

where, β_{calc}, β_{meas} and β_{inst} are the calculated, measured and instrumental broadening values, respectively.

$$d = \frac{0.9\lambda}{\beta_{calc}\cos\theta} \quad \text{(S2)}$$

where, d, λ and θ are the volume average of crystallite size, the wavelength of the radiation in angstrom and the diffraction peak position in radian, respectively.

Table S1: Calculated crystallite sizes of annealed precursors which are annealed at different temperatures.

Temperature (˚C)	**Average crystallite size (nm)**	
	In_2O_3	**CuO**
300	12.5	-
400	14.7	14.7

C. Cross-section SEM images of In_2O_3, CuO printed layers.

The oxide particles (especially, it is true for In_2O_3) are not clearly seen at the printed film surface. However, interestingly they are clearly visible in the cross-section SEM images. Here the cross-section SEM images of In_2O_3 and CuO layers (large-area solution casted films) are presented in order to compare and corroborate the crystallite size calculated using Scherer equation.

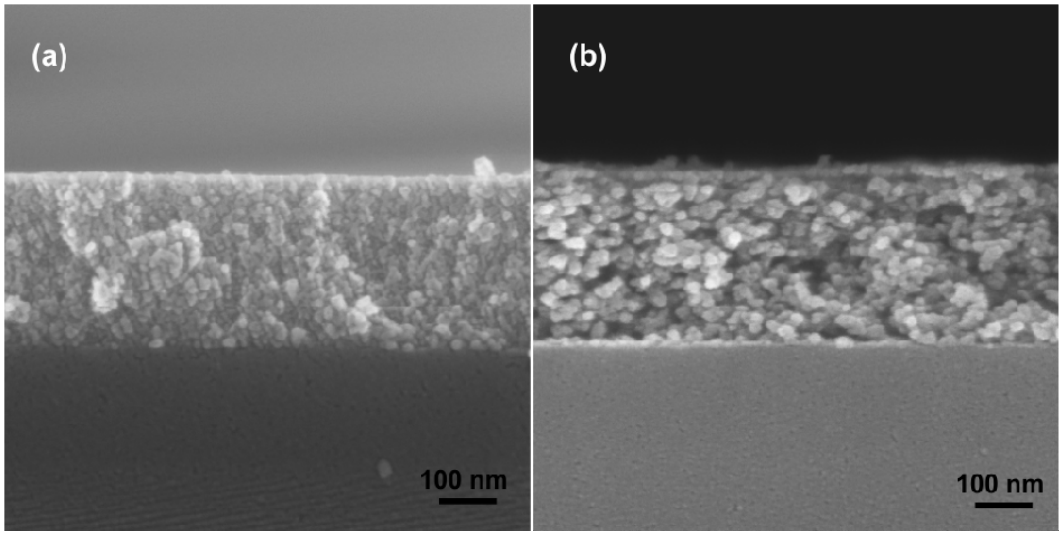

Figure S1. Cross-section SEM images of In_2O_3 and CuO layers.

D. XRD pattern of indium oxide precursor annealed at 230 °C

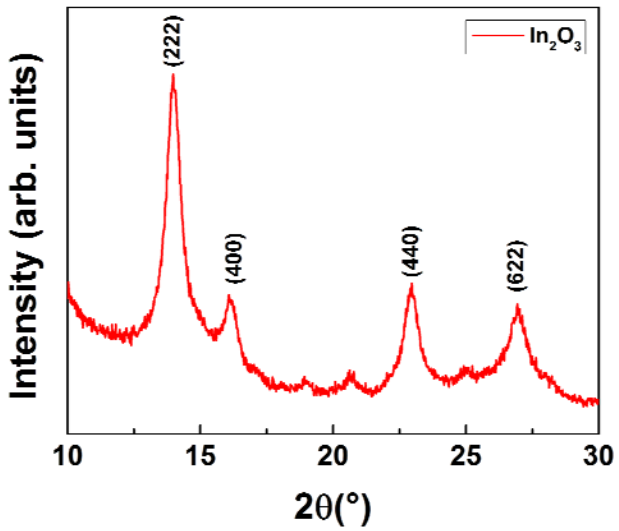

Figure S2: XRD pattern of indium oxide precursor annealed at 230 °C for 1 hr

E. Section and roughness analysis of AFM micrographs for the indium precursor annealed at 400 ˚C for 2 hr

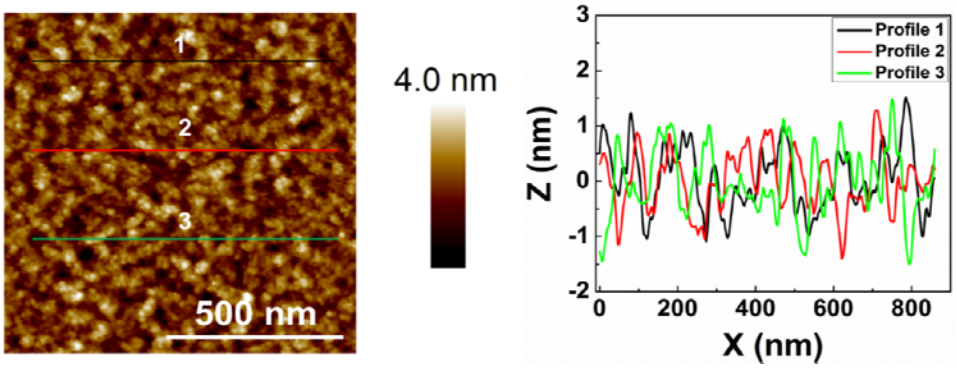

Figure S3: Section analysis of the indium oxide precursor annealed at 400 ˚C for 2 hr

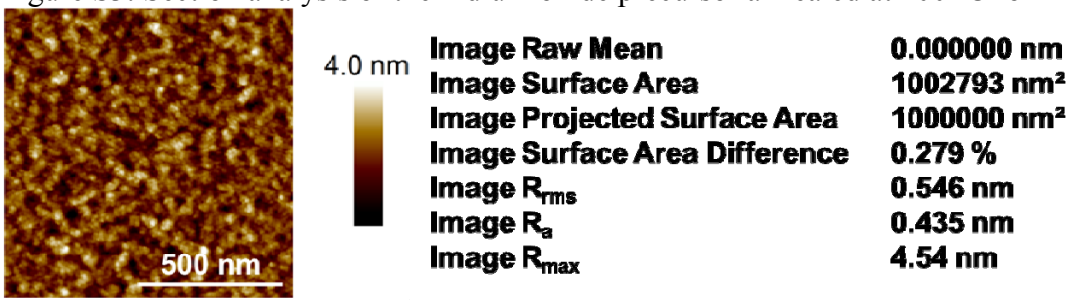

Figure S4: Roughness analysis of the indium oxide precursor annealed at 400 ˚C for 2 hr

F. Section and roughness analysis of AFM micrographs of the copper precursor annealed at 400 ˚C for 2 hr

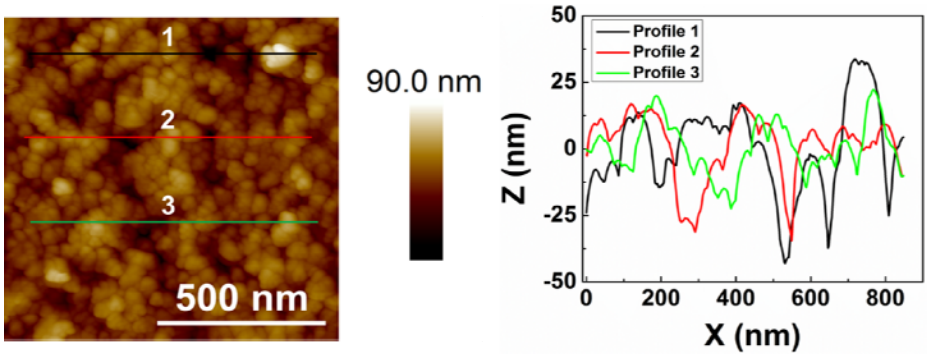

Figure S5: Section analysis of copper oxide precursor annealed at 400 ˚C for 2 hr

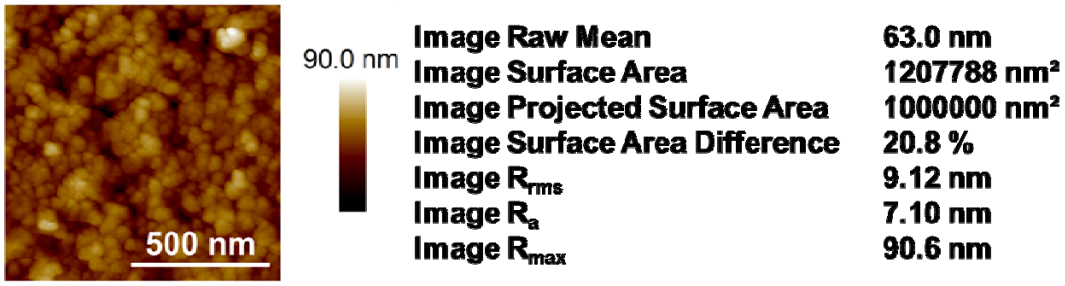

Figure S6: Roughness analysis of copper oxide precursor annealed at 400 ˚C for 2 hr

G. Transistor characteristics of indium acetate precursor which is annealed at 230 °C for 1hr

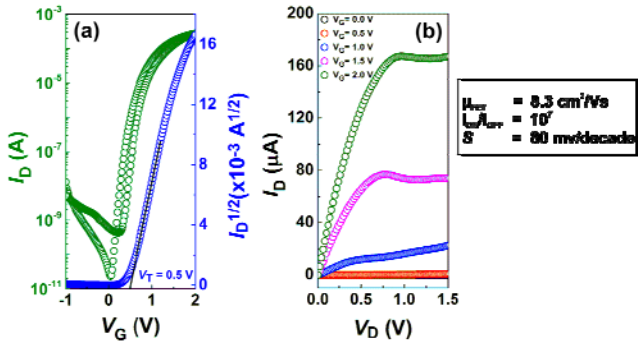

Figure S7. Transistor characteristics (a) Transfer and (b) I-V of Indium acetate precursor, annealed at 230 °C for 1hr.

H. Double layer capacitance (C_{DL}) calculation of indium oxide and copper oxide thin films

Two different approaches have been taken to calculate C_{DL} of In_2O_3 and CuO. In case of indium oxide, the double layer capacitance value has been estimated using an identical FET device with sputter ITO as the passive structures (drive electrodes) and observing the displacement currents with different gate voltage (V_G) scan rates, as shown in Figure S8a. An accurate estimation of C_{DL} following this process is only possible when the 'displacement current' is primarily resulting from the semiconducting active material and not from the high

conducting passive structures (*i.e.* source/drain electrodes). Next, the current density can be obtained by dividing the observed displacement current by the printed area.

A simple parallel plate capacitor model gives charge (Q) proportional to the voltage drop (V) across the capacitor, *i.e.*

$$Q = CV \tag{S3}$$

Differentiating equation (S3) with respect to t gives,

$$\frac{dQ}{dt} = C\frac{dV}{dt} \tag{S4}$$

where $\frac{dQ}{dt}$ is the said current density, *i.e.* the displacement current resulting from the unit area of the semiconductor and $\frac{dV}{dt}$ is the voltage scan rate, υ.

Therefore,

$$i = Cv \tag{S5}$$

Following equation (S5), the slope of Figure S8b gives the specific capacitance of the channel.

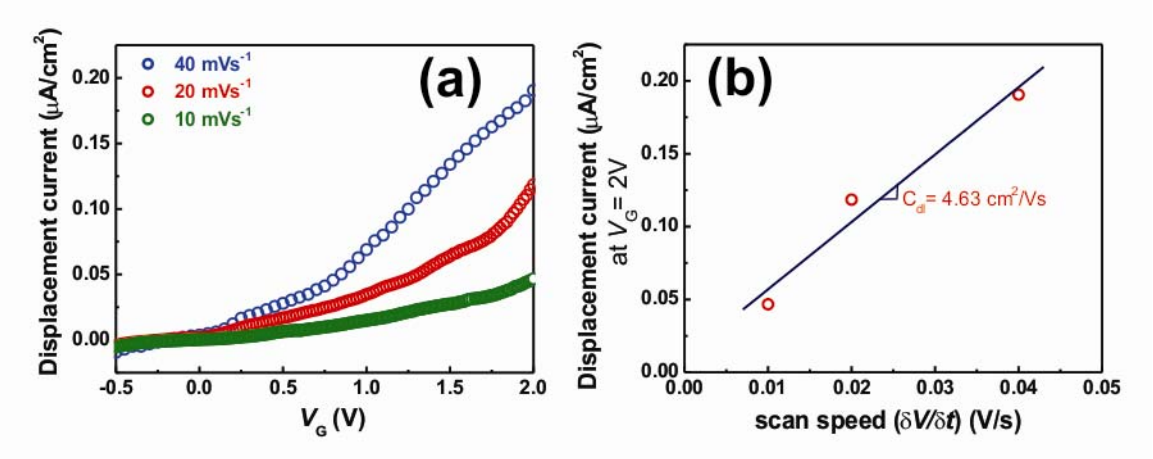

Figure S8. (a) Displacement current density at different gate voltage scan rates; (b) the displacement currents plotted against scan rates, the slope of the fit provides the double layer capacitance.

However, with CuO an identical approach is not possible. As already stated above, the calculation of C_{DL} from the displacement current is only possible when the parasitic current from the passive structures are negligible. However, here for CuO one must use pure metal (for example, we have used Pt) electrodes which results in considerable parasitic currents. Hence, a different approach is followed; large-area parallel plate capacitors are built with sputtered CuO thin films and with sputtered platinum as the counter electrode. Composite polymer electrolyte is solution casted in between the plate electrodes and dried in-situ to form all-solid capacitors. Cyclovoltammetry (CV) measurements are carried out to observe the displacement currents.

Copper oxide has low hole mobility; as a result, the electrolytic charging is incomplete even for a scan speed of 0.1 V/s, as can be seen in Fig. S9a. Therefore, in this case, the CV measurements are conducted at relatively low scan speeds 0.02-0.1 V/s. The calculated specific capacitance of copper oxide at a scan speed of 0.1 V/s (identical to the speed of FET measurements) is found 3.2μF/cm^2. Although low mobility, however, the specific capacitance is high enough, due to the fact that CuO has really high carrier concentration (close to 10^{19} cm^{-3}).[S2]

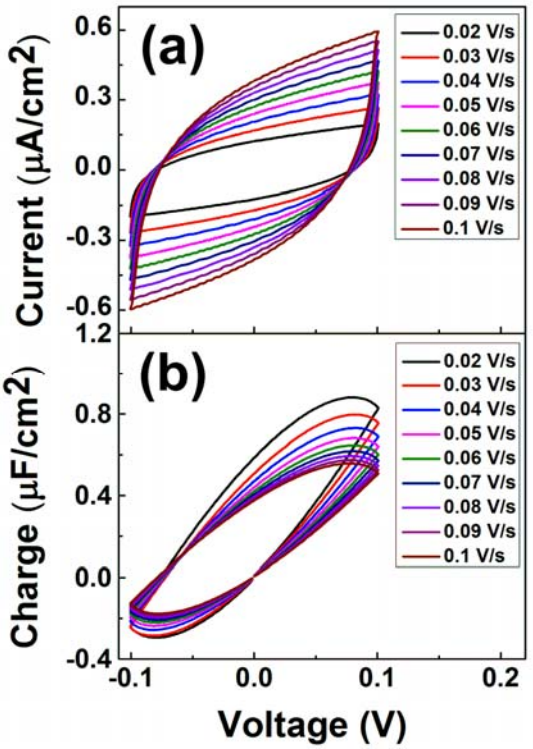

Figure S9: Cyclic voltammetry (CV) measurements at different scan rates are performed with sputtered copper oxide parallel plate capacitors; (a) displacement currents and (b) accumulated charge on the CuO electrodes, are presented.

I. Noise margin graphs of CMOS inverter

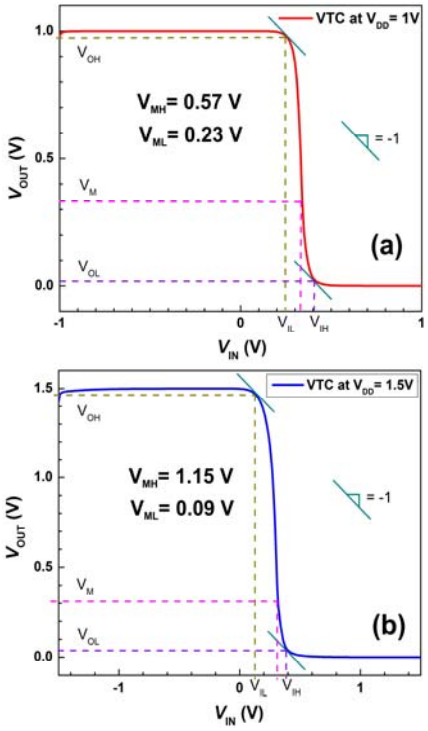

Figure S10: Noise margin graphs of CMOS inverter at (a) 1 V and (b) 1.5 V

J. Optical images of CMOS inverter and common source amplifier

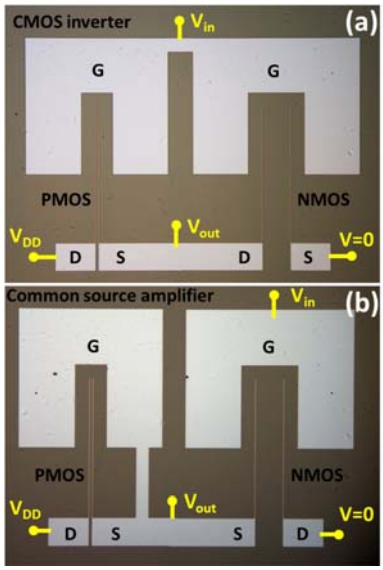

Figure S11: Optical images of (a) CMOS inverter and (b) common source amplifier

K. Rietveld refinement of the indium oxide and copper oxide thin films annealed at different temperatures

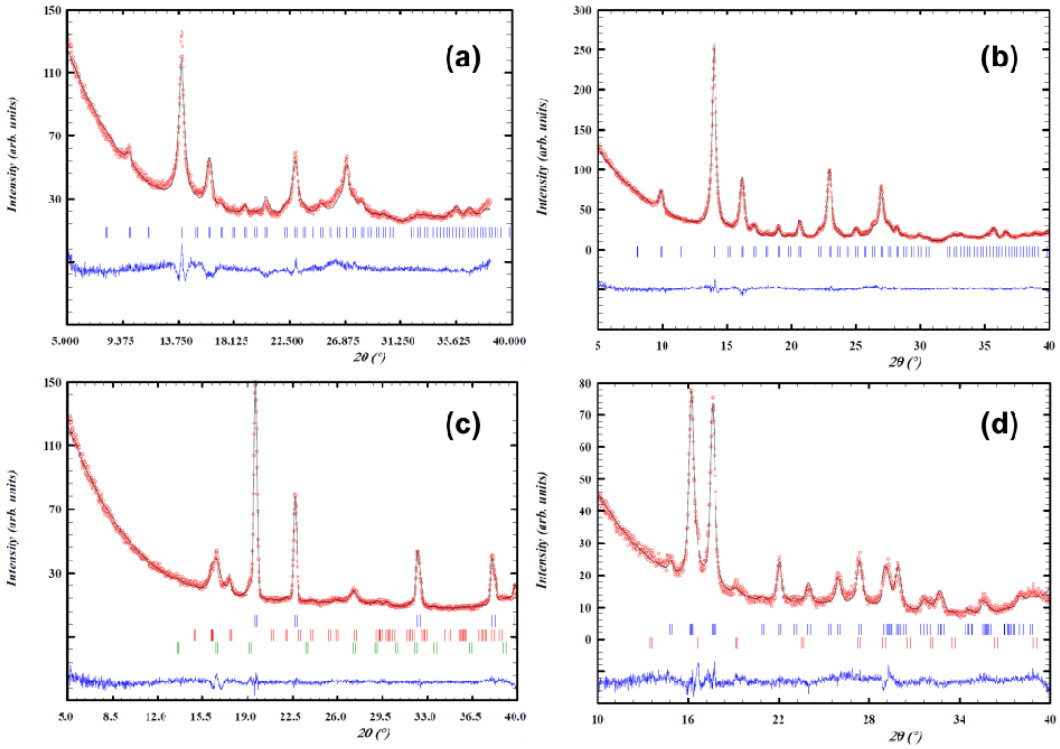

Figure S12: Rietveld refinement of the XRD data of printed indium oxide and cooper oxide thin films where the In_2O_3 precursors have been annealed at (a) 300 °C and (b) 400 °C, respectively; similarly, (c) and (d) corresponds to CuO precursors that have been heated to 300 °C and 400 °C, respectively.

Table S2 Quantitative phase analysis from the Rietveld fitting of the experimental data

Temperature (˚C)	**% fraction of phases**		
	Cu	**Cu_2O**	**CuO**
300	50	38	12
400	-	10	90

REFERENCES:
S1. Cullity, B. D. *Elements of X-ray Diffraction,* Addison-wesley publishing company, Inc., Massachusetts, **1956**, p. 262.
S2. A. Samokhvalov, N. Viglin, B. Gizhevskij, N. Loshkareva, V. Osipov, N. Solin and Y. P. Sukhorukov, *Zhurnal Eksperimentalnoi i Teoreticheskoi Fiziki*, **1993**, 103, 951-961.